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Sigma-Delta ADC on SOI Technology for Working at High Temperatures[1]

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Abstract—We consider the integrated circuit design and the measurement results of test crystals for the 12-bit sigma-delta analog-to-digital converter (ADC) based on 180 nm silicon-on-insulator (SOI) technology from X-FAB. The ADC processes input signals in the frequency range up to 100 kHz in the temperature range of –40…+175 °C with the supply voltage equal to 3.3 V and the modulator clock frequency equal to 10 MHz. The circuit consists of the 5-th order switched-capacitor low-pass pre-filter to limit the input signal spectrum, the cascade connection of the second order sigma-delta modulators, and the digital decimation filter to reduce the clock frequency by 48 times. The main blocks of cutoff filter and modulator are assembled according to the balanced scheme on integrators based on operational transconductance amplifiers with the unity gain bandwidth of 63 MHz. The dynamic element matching circuit is used to expand the dynamic range of converter. It reduces the level of nonlinear distortions in digital-to-analog converters in the feedback circuits of modulator. The value of the SINAD parameter is not worse than 68 dB for converting the signal with the differential amplitude equal to 500 mV at the frequency of 100 kHz.

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1. INTRODUCTION

As we know, sigma-delta analog-to-digital converters (ADCs) are widely used in various radio electronic devices [1], [2], however, an electronic component base is currently in demand for applications at high temperatures, for example, for distributed sensor systems [3]–[5]. In this paper we discuss the integrated circuit design and the measurement results of test crystals of sigma-delta ADC for operating in the extended temperature range, which is provided by the silicon-on-insulator (SOI) technology.

We select the X-FAB XT018 technology with the topological dimensions of 180 nm and the operating temperature range of –40…175 °C, while most of the known SOI technologies are designed for temperatures up to 125 °C [6]–[8]. The ADC has 12 bits and processes input signals in the frequency range up to 100 kHz and in the temperature range of –40…175 °C with the supply voltage equal to 3.3 V and the clock frequency of 10 MHz. According to the results of test crystals measurements the signal-to-noise and distortion ratio (SINAD) is not worse than 68 dB for the ADC input signal with the differential amplitude of 500 mV at the frequency of 100 kHz.

The work contains the following sections: the block diagram, layout and photo of the ADC crystal are presented in section 2; the schematic of the operational transconductance amplifier (OTA) is shown in section 3; the cutoff low-pass filter (LPF) is considered in section 4; the sigma-delta modulator (SDM) is

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CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

ADDITIONAL INFORMATION

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REFERENCES

1. A. Korotkov, D. Morozov, M. Pilipko, I. Piatak, and D. Budanov, "Analog-to-digital converters for wireless communication systems: design experience," *Electron. Sci. Technol. Bus.*, No. 2, 40 (2016). URL: https://www.electronics.ru/journal/article/5133.
2. V. S. Golub, "Sigma-delta modulator: Refinement of equivalent circuit and transfer function," *Radioelectron. Commun. Syst.* **53**, No. 6, 324 (2010). DOI: 10.3103/S0735272710060063.
3. A. S. Benediktov, N. A. Shelepin, P. V. Ignatov, A. A. Mikhailov, and A. G. Potupchik, "Investigating the dynamic characteristics of high-temperature SOI CMOS VLSIC elements," *Russ. Microelectron.* **47**, No. 3, 197 (2018). DOI: 10.1134/S1063739718030022.
4. J. Pathrose, C. Liu, K. T. C. Chai, and Y. Ping Xu, "A time-domain band-gap temperature sensor in SOI CMOS for higherature applications," *IEEE Trans. Circuits Syst. II Express Briefs* **62**, No. 5, 436 (2015). DOI: 10.1109/TCSII.2014.2386231.
5. M. Malits, I. Brouk, and Y. Nemirovsky, "Temperature sensing circuits in CMOS-SOI technology," in *2017 IEEE International Conference On Microwaves*, *Antennas*, *Communications and Electronic Systems*, *COMCAS 2017* (2017), Vol. 2017-Novem, pp. 1–5. DOI: 10.1109/COMCAS.2017.8244788.
6. L. Pedala, U. Sonmez, F. Sebastiano, K. A. A. Makinwa, K. Nagaraj, and J. Park, "An oxide electrothermal filter in standard CMOS," in *2016 IEEE SENSORS* (IEEE, 2016), pp. 1–3. DOI: 10.1109/ICSENS.2016.7808512.
7. H. Shan, J. Peterson, M.-S. Tsai, Y. Tang, N. J. Conrad, and S. Mohammadi, "A low power CMOS temperature sensor frontend for RFID tags," in *2018 IEEE 18th Topical Meeting On Silicon Monolithic Integrated Circuits In RF Systems* (*SiRF*) (IEEE, 2018), pp. 15–18. DOI: 10.1109/SIRF.2018.8304217.
8. F. Gerfers, N. Lotfi, E. Wittenhagen, H. Ghafarian, Y. Tian, and M. Runge, "Body-bias techniques in CMOS 22FDX® for mixed-signal circuits and systems," in *2019 26th IEEE International Conference On Electronics*, *Circuits And Systems* (*ICECS*) (IEEE, 2019), pp. 466–469. DOI: 10.1109/ICECS46596.2019.8964676.
9. A. S. Korotkov, M. M. Pilipko, D. V. Morozov, and J. Hauer, "Delta-sigma modulator with a 50-MHz sampling rate implemented in 0.18-μm CMOS technology," *Russ. Microelectron.* **39**, No. 3, 210 (2010). DOI: 10.1134/S106373971003008X.
10. J. M. de la Rosa, R. Schreier, K.-P. Pun, and S. Pavan, "Next-generation delta-sigma converters: Trends and perspectives," *IEEE J. Emerg. Sel. Top. Circuits Syst.* **5**, No. 4, 484 (2015). DOI: 10.1109/JETCAS.2015.2502164.
11. B. Razavi, "The delta-sigma modulator [A circuit for all seasons]," *IEEE Solid-State Circuits Mag.* **8**, No. 2, 10 (2016). DOI: 10.1109/MSSC.2016.2543061.
12. M. Sonika, D. D. Neema, and R. N. Patel, "Designs of multi-bit sigma delta modulator," *Radioelectron. Commun. Syst.* **59**, No. 6, 237 (2016). DOI: 10.3103/S0735272716060017.
13. A. S. Kozlov and M. M. Pilipko, "A Second-order sigma-delta modulator with a hybrid topology in 180nm CMOS," in *2020 IEEE Conference Of Russian Young Researchers In Electrical And Electronic Engineering* (*EIConRus*) (IEEE, 2020), pp. 144–146. DOI: 10.1109/EIConRus49466.2020.9039246.
14. G. Jovanovic Dolecek, J. R. Garcia Baez, and M. Laddomada, "Design of efficient multiplierless modified cosine-based comb decimation filters: Analysis and implementation," *IEEE Trans. Circuits Syst. I Regul. Pap.* **64**, No. 5, 1051 (2017). DOI: 10.1109/TCSI.2017.2653720.

15. Q. Huang, P. Wan, X. Xie, C. Wang, L. Su, and Z. Chen, "Digital filter design of a high resolution audio sigma-delta ADC," in *2018 12th IEEE International Conference On Anti-Counterfeiting*, *Security*, *And Identification* (*ASID*) (IEEE, 2018), pp. 208–211. DOI: 10.1109/ICASID.2018.8693141.
16. R. T. Baird, "Linearity enhancement of multibit ΔΣ A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.* **42**, No. 12, 753 (1995). DOI: 10.1109/82.476173.
17. V. O'Brien and B. Mullane, "High order mismatch shaping for low oversampling rates," *IEEE Trans. Circuits Syst. II Express Briefs* **67**, No. 1, 42 (2020). DOI: 10.1109/TCSII.2019.2904180.
18. J. R. Shakya and G. C. Temes, "Efficient calibration of feedback DAC in delta sigma modulators," *IEEE Trans. Circuits Syst. II Express Briefs* **67**, No. 5, 826 (2020). DOI: 10.1109/TCSII.2020.2984025.
19. V. I. Slyusar and M. Bondarenko, "Methods for estimating the ADC jitter in noncoherent systems," *Radioelectron. Commun. Syst.* **54**, No. 10, 536 (2011). DOI: 10.3103/S0735272711100037.
20. W. Kester, *The Data Conversion Handbook* (Newnes, Oxford, 2005). URL: https://www.analog.com/en/education/education-library/data-conversion-handbook.html#.