

Synthesis Method of Procedure for Odd-Order I/Q Demodulation Based on Replacing Multistage with Equivalent Single-Stage Demodulation Schemes

V. Slyusar^{1*} and P. Serdiuk^{2**}

¹Central Research Institute of Armaments and Military Equipment of the Armed Forces of Ukraine, Kyiv, Ukraine

²Heroes of Kruty Military Institute of Telecommunications and Information Technologies, Kyiv, Ukraine

*ORCID: [0000-0002-2912-3149](https://orcid.org/0000-0002-2912-3149), e-mail: swadim@ukr.net

**ORCID: [0000-0002-5497-456X](https://orcid.org/0000-0002-5497-456X)

Received September 9, 2017

Revised February 16, 2020

Accepted April 12, 2020

Abstract—A method of synthesis of odd-order I/Q demodulators based on replacing the multistage demodulation schemes with equivalent single-stage ones is proposed. The calculation of coefficients of single-stage odd-order I/Q demodulator, which is equivalent to multistage scheme in terms of the waveform of its amplitude-frequency characteristic (AFC), is based on the sample-wise analysis of the process of forming the response of the demodulator output stage that involves the sampling the harmonic signal voltages at the output of analog-to-digital converter (ADC). An example of synthesis of 11-sample former of quadrature components is considered for illustrating the application peculiarities of the method proposed for synthesis of odd-order I/Q demodulators. The comparative results of its AFC calculations are presented. The analytical description of the response of the specified unit in terms of the coefficients of even-order I/Q demodulators forming the multistage scheme has been derived. A number of regularities intrinsic to coefficients of odd-order I/Q demodulators was established, including the regularities characterizing the dependence of their dynamic range on values of weighting coefficients of the initial multistage scheme.

DOI: 10.3103/S0735272720050064

One of the important steps in processing the OFDM signals in receiving system is the formation of voltages of quadrature components of signal mixture. For simplifying the hardware implementation of the receiver analog segment, this operation can be performed in digital form using the so-called quadrature (I/Q) demodulators that are known as I/Q demodulators [1–4].

The possibility of replacing the multistage circuits of quadrature demodulators (Fig. 1) with single-stage equivalents is considered in [5]. This approach is based on achieving a rough match of amplitude-frequency characteristics (AFC) of single-stage schemes of high order I/Q demodulators and their multistage alternatives. For example, the AFC waveform of single-stage 16-sample I/Q demodulator with coefficients $a = 1$, $b = 79$, $c = 793$, $d = 2431$, $e = 3003$, $f = 1573$, $g = 299$, $h = 13$ and that of two-stage circuit with 8-sample I/Q demodulators having weighting coefficients $a = 1$, $b = 11$, $c = 15$, and $d = 5$ [4] almost coincide [6]. In this case, the two-stage scheme provides a gain in suppressing the out-of-band signals by 2–3 dB at the edges of transmission baseband.

In the general case, the specified similarity of AFC shapes is valid in comparing the two-stage M -sample and single-stage $2M$ -sample even-order I/Q demodulators while using the same method of calculating the coefficients. This fact stipulates the possibility of replacing the corresponding multistage schemes of generating the quadrature components of signals (quadrature demodulation) with equivalent single-stage schemes. However, the search for possible implementation of both the rough and identical replacement of specified alternative demodulation circuits with simultaneous synthesis of odd-order I/Q demodulators is of practical interest in selecting the specific implementation variants of I/Q demodulators.

The purpose of this paper is to develop the method for the calculation of coefficients of single-stage odd-order quadrature demodulator, the AFC of which will be identical in terms of its AFC waveform to that of the multistage scheme of building the even-order I/Q demodulators.

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

ADDITIONAL INFORMATION

The initial version of this paper in Russian is published in the journal “Izvestiya Vysshikh Uchebnykh Zavedenii. Radioelektronika,” ISSN 2307-6011 (Online), ISSN 0021-3470 (Print) on the link <http://radio.kpi.ua/article/view/S0021347020050064> with DOI: [10.20535/S0021347020050064](https://doi.org/10.20535/S0021347020050064).

REFERENCES

1. V. P. O'Neil, C. Ryan, and C. Weitzel, "Monolithic gallium arsenide I-Q demodulator," in *Proc. of Conf. on Microwave and Millimeter-Wave Monolithic Circuits*, 31 May-1 Jun. 1983, Dallas, USA (IEEE, 1983), Vol. 84, pp. 14–18. DOI: [10.1109/MCS.1984.1113618](https://doi.org/10.1109/MCS.1984.1113618).
2. C. Ziomek and P. Corredoura, "Digital I/Q demodulator," in *Proc. of IEEE Particle Accelerator Conf.*, 1995, Dallas, USA (IEEE, 2002), vol. 4, pp. 2663-2665. DOI: [10.1109/pac.1995.505652](https://doi.org/10.1109/pac.1995.505652).
3. D. Bernal, P. Closas, and J. A. Fernández-Rubio, "Digital I&Q demodulation in array processing: Theory and implementation," in *2008 16th European Signal Processing Conf.*, 25-29 Aug. 2008, Lausanne, Switzerland (IEEE, 2008). URI: <https://ieeexplore.ieee.org/document/7080413>.
4. J. E. Eklund and R. Arvidsson, "A multiple sampling, single A/D conversion technique for I/Q demodulation in CMOS," *IEEE J. Solid-State Circuits* **31**, No. 12, 1987 (Dec. 1996). DOI: [10.1109/4.545822](https://doi.org/10.1109/4.545822).
5. V. Slyusar and P. Serdjuk, "Multistage I/Q-demodulate OFDM signals at their one channel analog-digital transformation," *Zbirnyk Naukovykh Prats VITI NTUU KPI*, No. 1, 85 (KPI, Kyiv, 2013). URI: http://www.viti.edu.ua/files/zbk/2013/11_1_2013.pdf
6. V. Slyusar and E. Zhivilo, "The synthesis of equivalence digital filters for tandem decimation on base I/Q-demodulation," in *Proc. of 2017 4th Int. Sci.-Practical Conf. on Problems of Infocommunications Science and Technology*, PIC S&T, 10-13 Oct. 2017, Kharkiv, Ukraine (IEEE, 2018), pp. 449-451. DOI: [10.1109/INFOCOMMST.2017.8246436](https://doi.org/10.1109/INFOCOMMST.2017.8246436).
7. M. Mfana and A. N. Hasan, "Soft-core architecture for odd/even order sampling I/Q demodulator with dual-port block memory considerations," *Preprints* **2019**, 1 (Sep. 2019). DOI: [10.20944/preprints201909.0014.v1](https://doi.org/10.20944/preprints201909.0014.v1).
8. J. Mitra and T. K. Nayak, "An FPGA-based phase measurement system," *IEEE Trans. Very Large Scale Integr. Syst.* **26**, No. 1, 133 (Jan. 2018). DOI: [10.1109/TVLSI.2017.2758807](https://doi.org/10.1109/TVLSI.2017.2758807).
9. I. L. Syllaios, "Hybrid and $\Delta\Sigma$ programmable phase/frequency detector for IoT chipsets," *Proc. of IEEE Int. Symp. on Circuits and Systems*, 27-30 May 2018, Florence, Italy (IEEE, 2018), vol. 2018-May. DOI: [10.1109/ISCAS.2018.8351733](https://doi.org/10.1109/ISCAS.2018.8351733).
10. P. I. Puzyrev, K. V. Semenov, and S. A. Zavyalov, "Spurious-free dynamic range of cordic based digital quadrature demodulator," *Proc. of Int. Conf. of Young Specialists on Micro/Nanotechnologies and Electron Devices, EDM*, 29 Jun.-3 Jul. 2018, Erlagol, Russia (IEEE, 2018), vol. 2018-July, pp. 167-171. DOI: [10.1109/EDM.2018.8434980](https://doi.org/10.1109/EDM.2018.8434980).
11. J. Kang, et al., "A system-on-chip solution for point-of-care ultrasound imaging systems: Architecture and ASIC implementation," *IEEE Trans. Biomed. Circuits Syst.* **10**, No. 2, 412 (Apr. 2016). DOI: [10.1109/TBCAS.2015.2431272](https://doi.org/10.1109/TBCAS.2015.2431272).
12. A. Mandal, R. Mishra, M. R. Nagar, "Implementation of complex digital PLL for phase detection in software defined radar," *Radioelectron. Commun. Syst.* **59**, No. 4, 151 (2016). DOI: [10.3103/S0735272716040014](https://doi.org/10.3103/S0735272716040014).