ISSN 0735-2727, Radioelectronics and Communications Systems, 2020, Vol. 63, No. 2, pp. 96–104. © Allerton Press, Inc., 2020.
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Studying Generation Modes of Linearized Artificial Neurons Based on FPGA Architecture Hardware Implementation

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Received February 19, 2019
Revised January 7, 2020
Accepted January 30, 2020

Abstract—This paper describes the development of embedded software for the implementation and testing of the artificial multistable neuron model's basic behavior with the help of the hardware architecture of programmable logic integrated circuits (FPGA). The real behavior and function of the biological neuron with linearized activation characteristics are investigated and implemented in the programming language VHD. The base model is a three-stable neuron with three asymmetric dendrites. To develop a hardware model, a computational mathematical model of a neuron is used, based on which a corresponding discrete model is synthesized. The model consists of the following modules: an input block, a timer, a clock generator, a threshold element, and an output signal generator. It is shown that the implemented system allows synthesizing a neural model with a predetermined number of stable discrete states, with the neuron changing its stable state depending on the input vector. Each stable state corresponds to the output function of the neuron. The developed model of artificial neurons was implemented on the DIGILENT BASYS II SPARTAN-3E XC3S100E FPGA kit in the WebPACKTM ISE 13.3 environment. Resulting neuron output generation modes relation from input sequences and structure parameters were studied. The results of the work allow investigating high-speed neural networks with a dynamic structure using FPGA, which can be used for a wide range of modern tasks such as recognition, classification of patterns and development of elements of artificial intelligence.

DOI: 10.3103/S0735272720020053

1. PROBLEM BACKGROUND

Considerable work has been done on the development and implementation of hardware neurocomputers since the 2000s. However, most of these efforts can be considered unsuccessful: none of the systems was widely used. The lack of success is because the previous work was almost entirely focused on the development of neurocomputers [1] that are built on the application-specific integrated circuit (ASIC) technology. However, this technology has never been sufficiently developed and competitive for large-scale deployment [2] for areas such as neural networks.

The significant improvement of modern technologies has opened a new way. The potential and performance of existing FPGAs are such that they provide a much more realistic alternative. FPGA-based neurocomputers can be the basis for the mass implementation of parallel distributed data processing systems. The main task in all forms of parallel computing is to translate as many processes as possible into hardware for their rapid execution in parallel mode and with minimal energy costs.

Moreover, the model of a neuron or neural network is a dynamic structure where changes, even structural ones, can occur [3, 4]. The flexible FPGA structures become the most attractive for modeling neural networks and allow modeling the behavior of artificial neurons with biological similarity in real-time.

The main limitation of the software implementation of neurons, neural networks, and pattern recognition systems is the consecutive execution of calculations. Compared to any modern microcontroller, FPGAs have the reconfiguration property and very low power consumption while maintaining high power and small linear dimensions [5]. Delayed execution of an algorithm of several milliseconds can be significant for use, for example, in medical diagnostics.

Reconfigured FPGA-based computations are well-suited for the implementation of neural structures because they utilize parallelism and can be quickly reconfigured according to input weights and neuronal

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

ADDITIONAL INFORMATION

The initial version of this paper in Russian is published in the journal "Izvestiya Vysshikh Uchebnykh Zavedenii. Radioelektronika," ISSN 2307-6011 (Online), ISSN 0021-3470 (Print) on the link http://radio.kpi.ua/article/view/S0021347020020053 with DOI: 10.20535/S0021347020020053.

REFERENCES

1. J. A. Bailey, R. Wilcock, P. R. Wilson, and J. E. Chad, "Behavioral simulation and synthesis of biological neuron systems using synthesizable VHDL," *Neurocomputing* **74**, No. 14-15, 2392 (Jul. 2011). DOI: 10.1016/j.neucom.2011.04.001.
2. P. Wilson, B. Metcalfe, J. Graham-Harper-Cater, and J. A. Bailey, "A reconfigurable architecture for real-time digital simulation of neurons," in *2017 Intelligent Systems Conference*, IntelliSys 2017 (2018), vol. 2018-January, pp. 66–75. DOI: 10.1109/IntelliSys.2017.8324340.
3. R. R. Borges et al., "Effects of the spiketiming-dependent plasticity on the synchronisation in a random Hodgkin-Huxley neuronal network," *Commun. Nonlinear Sci. Numer. Simul.* **34**, 12 (2016). DOI: 10.1016/j.cnsns.2015.10.005.
4. J. E. G-H-Cater, C. T. Clarke, B. W. Metcalfe, and P. R. Wilson, "A reconfigurable architecture for implementing locally connected neural arrays," in *Advances in Intelligent Systems and Computing* (2019), vol. 857, pp. 76–92. DOI: 10.1007/978-3-030-01177-2_6.
5. I. Sahin and N. K. Saritekin, "A data path design tool for automatically mapping artificial neural networks on to FPGA-based systems," *J. Electr. Eng. Technol*. **11**, No. 5, 1466 (Sep. 2016). DOI: 10.5370/JEET.2016.11.5.1466.
6. E. Z. Mohammed and H. K. Ali, "Hardware Implementation of Artificial Neural Network Using Field Programmable Gate Array," *Int. J. Comput. Theory Eng.*, 780 (2013). DOI: 10.7763/ijcte.2013.v5.795.
7. F. Pérez-Peña, A. Morgado-Estévez, and A. Linares-Barranco, "Inter-spikes-intervals exponential and gamma distributions study of neuron firing rate for SVITE motor control model on FPGA," *Neurocomputing* **149**, No. PB, 496 (Feb. 2015). DOI: 10.1016/j.neucom.2014.08.024.
8. F. Akopyan et al., "TrueNorth: Design and Tool Flow of a 65 mW 1 Million Neuron Programmable Neurosynaptic Chip," *IEEE Trans. Comput. Des. Integr. Circuits Syst.* **34**, No. 10, 1537 (Oct. 2015). DOI: 10.1109/TCAD.2015.2474396.
9. W. Rawat and Z. Wang, "Deep convolutional neural networks for image classification: A comprehensive review," *Neural Computation* **29**, No. 9, 2352 (01-Sep-2017). DOI: 10.1162/NECO_a_00990.
10. Y. Ghelamallah, D. Chalabi, A. Saïdane, and Z. Chalabi, "Implementation on FPGA circuit of the medical image processing algorithms within the framework of assistance to the medical diagnosis," *Int. Rev. Comput. Softw.* **10**, No. 10, 987 (2015). DOI: 10.15866/irecos.v10i10.7155.
11. A. Podili, C. Zhang, and V. Prasanna, "Fast and efficient implementation of Convolutional Neural Networks on FPGA," in *Proceedings of the International Conference on Application-Specific Systems, Architectures and Processors* (2017), pp. 11–18. DOI: 10.1109/ASAP.2017.7995253.
12. S. M. Korogod and D. V. Chernetchenko, "Nature of electrical tristability in a neuron model with bistable asymmetrical dendrites," *Neurophysiology* **40**, No. 5-6, 412 (2008). DOI: 10.1007/s11062-009-9067-2.
13. Y. M. Snizhko and D. V. Chernetchenko, "Dynamics of electrical potentials of neuron networks models with non-linear activation functions," *Vestnik DNU* **20**, No. 2, 50 (2012).
14. A. Alaburda, M. Alaburda, A. Baginskas, A. Gutman, and G. Svirskis, "Criteria of bistability of the cylindrical dendrite with a variable negative slope of the N-shaped current-voltage membrane characteristic," *Biofizika* **46**, No. 2, 340 (2001).
15. S. Yin et al., "A High Energy Efficient Reconfigurable Hybrid Neural Network Processor for Deep Learning Applications," *IEEE J. Solid-State Circuits* **53**, No. 4, 968 (Apr. 2018). DOI: 10.1109/JSSC.2017.2778281.