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Digitally-Controlled Ring Oscillator for Wide Tuning Range Applications

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Abstract—In this paper, two digitally-controlled ring oscillators (DROs) with similar structure but different constructive cells have been proposed. These proposed DROs include of 5 stages, and each stage contains 10 parallel delay cells. In addition, each stage has fine and coarse parts for adjusting the output frequency. The proposed designs have a wide frequency range and high frequency. The frequency range of the first DRO changes from 1.566 to 20.25 GHz (92.6%) and for the second DRO, its frequency is from 2.218 to 22.86 GHz (90.31%). By considering all possible digital codes for fine and coarse stages, the power consumption of the first DRO changes from 1.1 to 13.64 mW, while this value for the second DRO varies from 144.1 μW to 1.76 mW. The phase noise of the first DRO at the center frequency of 20.25 GHz and the 1 MHz offset is equal to –76.24 dBc/Hz, and at 10 MHz offset the phase noise is equal to –104 dBc/Hz. The phase noise of the second DRO at the center frequency of 22.86 GHz and the 1 MHz offset is equal to –66.64 dBc/Hz, and at the 10 MHz offset the phase noise is equal to –95.39 dBc/Hz. The proposed DROs have been simulated by using the Cadence software in TSMC 65nm CMOS technology and 1.2 V power supply.

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1. INTRODUCTION

The phase locked loops (PLLs) are widely used in many communication systems, including frequency synthesizers, clock and data recovery systems, on-chip clock generators and so on [1–7]. These phase locked loops can be designed in three forms including analog (PLL), digital (DPLL) and all-digital (ADPLL) designs.

The analog types are more sensitive to process, voltage and temperature variations (PVT), and they have a larger area and power consumption as compared to ADPLL [5, 8–10]. Moreover, when the technology changes, an analog PLL must be redesigned, and this is one of the major defects of the analog PLL [11].

Furthermore, in the case of deep submicron technology, an analog PLL leakage current increases. Therefore, in order to prevent this phenomenon, the supply voltage should be reduced, which leads to the rise of phase noise and degradation of performance [12].

On the other hand, ADPLLs are more suitable for SOC (system-on-chip) applications than analog PLLs. Additionally, ADPLLs can be implemented with automated CAD tools that reduces design time. Another advantage of ADPLLs is that they have the ability to integrate and modify applications and simplify the fabrication process [13].

ADPLLs also have a good stability against noise in the CMOS nanometer scale, and because they are composed of digital components, they are less sensitive to external noise [5]. In addition to the above, ADPLLs have high testability and stability, short lock-in time and small area [14].

One of important blocks of PLLs is an oscillator. Ther are two types of oscillators: voltage-controlled oscillator (VCO) and digitally-controlled oscillator (DCO).

VCO can be applied in analog PLL, since the continuous variations of its control voltage change the frequency, while DCO, where the control codes change its frequency, is the primary core of ADPLL [2, 15–19].

There are different structures for DCO including the LC tank and the ring (DRO) structure that are wider used in integrated circuits due to their suitability. On the other hand, the LC tank oscillators are the best

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

ADDITIONAL INFORMATION

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