Design and Analysis of Wide Tuning Range Ring VCO in 65nm CMOS Technology

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Abstract—In this article a ring voltage controlled oscillator (VCO) with four stages consisting of differential delay cells with two control voltages is proposed. This VCO uses the dual-delay loop technique for high operation frequency. Each delay cell of the proposed VCO includes two pairs of PMOS and NMOS cross-coupled load transistors to form a latch. The strength of the added latch and the operation frequency are adjusted with a pair cross-coupled NMOS pass transistors. Furthermore, to adjust the frequency of the proposed VCO in higher frequencies, the effect of the secondary path of this VCO is changed. The proposed VCO is simulated in 65nm TSMC CMOS technology in Cadence software and 1.2 V supply voltage. The wide tuning range of the proposed VCO varies from 4.25 to 21.31 GHz (80.07%), its power is 12.36 mW at 4.25 GHz frequency. The phase noise is −90.47 dBc/Hz at 1 MHz offset frequency and −117.4 dBc/Hz at 10 MHz offset frequency from 4.25 GHz while its area is 535.99 mm².

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1. INTRODUCTION

Phase-locked loop (PLL) is the essential block in wireless and communication systems to track the phase and frequency of the input data. It composed of different parts and voltage controlled oscillator (VCO) is vital part of it [1, 2].

Two widely used VCOs are LC VCOs and ring VCOs. LC VCOs have the high resolution and frequency but they suffer from the limited tuning range and large chip area. On the other hand, because the ring-VCOs have many advantages such as the wide tuning range, low chip area, easy integration, multiphase clock and low power consumption, it is a critical component that has been widely used in analog and digital applications. However, ring-VCOs suffer from the poor phase noise performance and low resolution [3–7].

Ring VCOs are divided into two types of single-ended ring VCO (SERO) and differential ring VCO (DRO). Both of them consist of several latency stages and the output of the last stage is connected to the input of the first stage. Every stage should add \((180/N)°\) to the phase where \(N\) is the number of stages. The simplest ring VCO is a loop, which consists of three basic inverters, has the highest oscillation frequency and minimum power dissipation.

SEROs compared to DROs consume less area but have more noise, therefore, they are less efficient and can only have odd number of stages. While DROs have better immunity to common mode noise and are more appropriate to eliminate the need for pass and coupling capacitors. Also they can have odd or even number of stages and they have lower swing and 50% duty cycle at the output. Furthermore the DRO with the even number of stages can be used for multi-phase outputs [8–14].

The DRO structure includes many tradeoffs between phase noise, frequency tuning range, maximum frequency, power dissipation, occupied area and multiphase output signals [15, 16]. The application scope which of the parameters are more important for a given VCO. Therefore, in each VCO, different methods are applied to improve more important parameters, while trying to maintain other parameters.

The dual-delay loop in [17] is such a method that is used to increase the operation frequency. In this method, there are two different delay paths such that the main path has more delay than the secondary path. Usually the secondary path is applied to the input PMOS transistors gate of the delay cell. Subharmonic
CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

ADDITIONAL INFORMATION

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