ISSN 0735-2727, Radioelectronics and Communications Systems, 2019, Vol. 62, No. 5, pp. 232–240. © Allerton Press, Inc., 2019.
Russian Text © The Author(s), 2019, published in Izvestiya Vysshikh Uchebnykh Zavedenii, Radioelektronika, 2019, Vol. 62, No. 5, pp. 287–296.

Design and Analysis of Wide Tuning Range Ring VCO in 65nm CMOS Technology

Shirin Askari*, Mohsen Saneei, and Sanaz Salem*****

Shahid Bahonar University of Kerman, Kerman, Iran
**ORCID: 0000-0002-4924-2495, e-mail: shirin.askari@eng.uk.ac.ir*
***ORCID: 0000-0002-2722-6064, e-mail: msaneei@uk.ac.ir*
****ORCID: 0000-0003-4829-5859, e-mail: s.salem@eng.uk.ac.ir*

Received January 8, 2019
Revised March 27, 2019
Accepted March 29, 2019

Abstract—In this article a ring voltage controlled oscillator (VCO) with four stages consisting of differential delay cells with two control voltages is proposed. This VCO uses the dual-delay loop technique for high operation frequency. Each delay cell of the proposed VCO includes two pairs of PMOS and NMOS cross-coupled load transistors to form a latch. The strength of the added latch and the operation frequency are adjusted with a pair cross-coupled NMOS pass transistors. Furthermore, to adjust the frequency of the proposed VCO in higher frequencies, the effect of the secondary path of this VCO is changed. The proposed VCO is simulated in 65nm TSMC CMOS technology in Cadence software and 1.2 V supply voltage. The wide tuning range of the proposed VCO varies from 4.25 to 21.31 GHz (80.07%), its power is 12.36 mW at 4.25 GHz frequency. The phase noise is –90.47 dBc/Hz at 1 MHz offset frequency and –117.4 dBc/Hz at 10 MHz offset frequency from 4.25 GHz while its area is 535.99 μm^2.

DOI: 10.3103/S0735272719050054

1. INTRODUCTION

Phase-locked loop (PLL) is the essential block in wireless and communication systems to track the phase and frequency of the input data. It composed of different parts and voltage controlled oscillator (VCO) is vital part of it [1, 2].

Two widely used VCOs are *LC* VCOs and ring VCOs. *LC* VCOs have the high resolution and frequency but they suffer from the limited tuning range and large chip area. On the other hand, because the ring-VCOs have many advantages such as the wide tuning range, low chip area, easy integration, multiphase clock and low power consumption, it is a critical component that has been widely used in analog and digital applications. However, ring-VCOs suffer from the poor phase noise performance and low resolution [3–7].

Ring VCOs are divided into two types of single-ended ring VCO (SERO) and differential ring VCO (DRO). Both of them consist of several latency stages and the output of the last stage is connected to the input of the first stage. Every stage should add (180/*N*)° to the phase where *N* is the number of stages. The simplest ring VCO is a loop, which consists of three basic inverters, has the highest oscillation frequency and minimum power dissipation.

SEROs compared to DROs consume less area but have more noise, therefore, they are less efficient and can only have odd number of stages. While DROs have better immunity to common mode noise and are more appropriate to eliminate the need for pass and coupling capacitors. Also they can have odd or even number of stages and they have lower swing and 50% duty cycle at the output. Furthermore the DRO with the even number of stages can be used for multi-phase outputs [8–14].

The DRO structure includes many tradeoffs between phase noise, frequency tuning range, maximum frequency, power dissipation, occupied area and multiphase output signals [15, 16]. The application scope which of the parameters are more important for a given VCO. Therefore, in each VCO, different methods are applied to improve more important parameters, while trying to maintain other parameters.

The dual-delay loop in [17] is such a method that is used to increase the operation frequency. In this method, there are two different delay paths such that the main path has more delay than the secondary path. Usually the secondary path is applied to the input PMOS transistors gate of the delay cell. Subharmonic

CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

ADDITIONAL INFORMATION

The initial version of this paper in Russian is published in the journal "Izvestiya Vysshikh Uchebnykh Zavedenii. Radioelektronika," ISSN 2307-6011 (Online), ISSN 0021-3470 (Print) on the link http://radio.kpi.ua/article/view/S0021347019050054 with DOI: 10.20535/S0021347019050054.

REFERENCES

1. N. K. Mendhe, M. N. Thakare, G. D. Korde, "High frequency power optimized ring voltage controlled oscillator for 65nm CMOS technology-Review," *Int. J. Eng. Trends Tech.* **8**, No. 3, 127 (2014). DOI: 10.14445/22315381/IJETT-V8P223.
2. A. Mandal, R. Mishra, M. R. Nagar, "Implementation of complex digital PLL for phase detection in software defined radar," *Radioelectron. Commun. Syst.* **59**, No. 4, 151 (2016). DOI: 10.3103/S0735272716040014.
3. Z. Chen, M. Wang, J.-X. Chen, W.-F. Liang, P.-P. Yan, J.-F. Zhai, Wei Hong, "Linear CMOS LC-VCO based on triple-coupled inductors and its application to 40-GHz phase-locked loop," *IEEE Trans. Microwave Theory Tech.* **65**, No. 8, 2977 (2017). DOI: 10.1109/TMTT.2017.2663401.
4. R. Islam, A. N. K. Suprotik, S. M. Zia Uddin, M. T. Amin, "Design and analysis of 3 stage ring oscillator based on MOS capacitance for wireless applications," *Proc. of Int. Conf. on Electrical*, *Computer and Communication Engineering*, 16-18 Feb. 2017, Cox's Bazar, Bangladesh (IEEE, 2017), pp. 723-727. DOI: 10.1109/ECACE.2017.7912998.
5. W.-T. Lee, J. Shim, J. Jeong, "Design of a three-stage ring-type voltage-controlled oscillator with a wide tuning range by controlling the current level in an embedded delay cell," *Microelectronics J.* **44**, No. 12, 1328 (2013). DOI: 10.1016/j.mejo.2013.09.003.
6. J. Yin, P.-I. Mak, F. Maloberti, R. P. Martins, "A time-interleaved ring-VCO with reduced 1/f3 phase noise corner, extended tuning range and inherent divided output," *IEEE J. Solid-State Circuits* **51**, No. 12, 2979 (2016). DOI: 10.1109/JSSC.2016.2597847.
7. X. Zhang, A. B. Apsel, "A low-power, process-and-temperature-compensated ring oscillator with addition-based current source," *IEEE Trans. Circuits Systems I: Regular Papers* **58**, No. 5, 868 (2011). DOI: 10.1109/TCSI.2010.2092110.
8. M. S. S. Kumar, M. Aarthy, "A 2.8 GHz low power high tuning voltage controlled ring oscillator," *Int. J. Eng. Advanced Tech.* **3**, No. 4, 2249 (2014).

9. S. Suman, K. G. Sharma, P. K. Ghosh, "Analysis and design of current starved ring VCO," *Proc. of Int. Conf. on Electrical*, *Electronics*, *and Optimization Techniques*, 3-5 Mar. 2016, Chennai, India (IEEE, 2016), pp. 3222-3227. DOI: 10.1109/ICEEOT.2016.7755299.
10. A. Ramazani, S. Biabani, G. Hadidi, "CMOS ring oscillator with combined delay stages," *AEU - Int. J. Electronics Commun.* **68**, No. 6, 515 (2014). DOI: 10.1016/j.aeue.2013.12.008.
11. J. Johnson, M. Ponnambalam, P. V. Chandramani, "Comparison of tunability and phase noise associated with injection locked three staged single and differential ended VCOs in 90nm CMOS," *Proc. of 2017 Fourth Int. Conf. on Signal Processing*, *Communication and Networking*, 16-18 Mar. 2017, Chennai, India (IEEE, 2017), pp. 1-4. DOI: 10.1109/ICSCN.2017.8085700.
12. H. Ghonoodi, H. Miar-Naimi, M. Gholami, "Analysis of frequency and amplitude in CMOS differential ring oscillators," *Integration* **52**, 253 (2016). DOI: 10.1016/j.vlsi.2015.07.004.
13. S. Salem, M. Tajabadi, M. Saneei, "The design and analysis of dual control voltages delay cell for low power and wide tuning range ring oscillators in 65nm CMOS technology for CDR applications," *AEU - Int. J. Electronics Commun.* **82**, 406 (2017). DOI: 10.1016/j.aeue.2017.10.012.
14. A. Sharma, Saurabh, S. Biswas, "A low power CMOS voltage controlled oscillator in 65 nm technology," *Proc. of Int. Conf. on Computer Communication and Informatics*, 3-5 Jan. 2014, Coimbatore, India (IEEE, 2014), pp. 1-5. DOI: 10.1109/ICCCI.2014.6921794.
15. G. Jovanovic, M. Stojcev, Z. Stamenkovic, "A CMOS voltage controlled ring oscillator with improved frequency stability," *Scientific Publications of the State University of Novi Pazar*, *Series A: Applied Mathematics*, *Informatics and mechanics*, Vol. 2, p. 1-9 (2010).
16. T. Kackar, S. Suman, P. K. Ghosh, "Differential voltage controlled ring oscillators—A review," *Proc. of Int. Conf. on Communication and Networks* **508**, 571 (2017). DOI: 10.1007/978-981-10-2750-5_59.
17. M.-L. Sheu, Y.-S. Tiao, L.-J. Taso, "A 1-V 4-GHz wide tuning range voltage-controlled ring oscillator in 0.18 μm CMOS," *Microelectronics J.* **42**, No. 6, 897 (2011). DOI: 10.1016/j.mejo.2011.03.015.
18. S.-y. Lee, S. Amakawa, N. Ishihara, K. Masu, "2.4-10 GHz low-noise injection-locked ring voltage controlled oscillator in 90 nm complementary metal oxide semiconductor," *Japanese J. Appl. Phys.* **50**, No. 4S, 04DE03 (2011). DOI: 10.1143/JJAP.50.04DE03.
19. M. Parvizi, A. Khodabakhsh, A. Nabavi, "Low-power high-tuning range CMOS ring oscillator VCOs," *Proc. of IEEE Int. Conf. on Semiconductor Electronics*, 25-27 Nov. 2008. Johor Bahru, Malaysia (IEEE, 2008), pp. 40-44. DOI: 10.1109/SMELEC.2008.4770273.
20. Y.-S. Tiao, M.-L. Sheu, "Full range voltage-controlled ring oscillator in 0.18μm CMOS for low-voltage operation," *Electron. Lett.* **46**, No. 1, 30 (2010). DOI: 10.1049/el.2010.2542.
21. S. Min, T. Copani, S. Kiaei, B. Bakkaloglu, "A 90-nm CMOS 5-GHz ring-oscillator PLL with delay-discriminator-based active phase-noise cancellation," *IEEE J. Solid-State Circuits* **48**, No. 5, 1151 (2013). DOI: 10.1109/JSSC.2013.2252515.
22. K.-H. Cheng, S.-C. Kuo, C.-M. Tu, "A low noise, 2.0 GHz CMOS VCO design," *Proc. of IEEE 46th Midwest Symp. on Circuits and Systems*, 27-30 Dec. 2003, Cairo, Egypt (IEEE, 2003), pp. 205-208. DOI: 10.1109/MWSCAS.2003.1562254.
23. V. Thakur, V. Verma, "Low power consumption differential ring oscillator," *Int. J. Electronics Commun. Eng.* **6**, No. 1, 81 (2013). URI: http://www.irphouse.com/ijece/ijecev6n1_09.pdf.
24. G. Haijun, S. Lingling, K. Xiaofei, L. Liheng, "A low-phase-noise ring oscillator with coarse and fine tuning in a standard CMOS process," *J. Semiconductors* **33**, No. 7, 075004 (2012). DOI: 10.1088/1674-4926/33/7/075004.
25. A. C. Demartinos, A. Tsimpos, S. Vlassis, S. Sgourenas, G. Souliotis, "A 3GHz VCO suitable for MIPI M-PHY serial interface," *Proc. of 10th Int. Conf. on Design & Technology of Integrated Systems in Nanoscale Era*, 21-23 Apr. 2015, Naples, Italy (IEEE, 2015), pp. 1-6. DOI: 10.1109/DTIS.2015.7127353.
26. J.-M. Kim, S. Kim, I.-Y. Lee, S.-K. Han, S.-G. Lee, "A low-noise four-stage voltage-controlled ring oscillator in deep-submicrometer CMOS technology," *IEEE Trans. Circuits Systems II: Express Briefs* **60**, No. 2, 71 (2013). DOI: 10.1109/TCSII.2012.2235734.
27. J. Jalil, M. B. I. Reaz, M. A. M. Ali, "CMOS differential ring oscillators: Review of the performance of CMOS ROs in communication systems," *IEEE Microwave Mag.* **14**, No. 5, 97 (2013). DOI: 10.1109/MMM.2013.2259401.
28. S. Yoo, J. J. Kim, J. Choi, "A 2-8 GHz wideband dually frequency-tuned ring-VCO with a scalable K_{VCO}," *IEEE Microwave Wireless Components Lett.* **23**, No. 11, 602 (2013). DOI: 10.1109/LMWC.2013.2280641.