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High Efficiency Cross-Coupled Charge Pump Circuit with Four-Clock Signals[1]

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Abstract—A fully integrated cross-coupled charge pump circuit for boosting dc-to-dc converter applications with four-clock signals has been proposed. With the new clock scheme, this charge pump eliminates all of the reversion power loss and reduces the ripple voltage. In addition, the largest voltage differences between the terminals of all transistors do not exceed the power supply voltage for solving the gate-oxide overstress problem in the conventional charge pump circuits and enhancing the reliability. This proposed charge pump circuit does not require any extra level shifter; therefore, the power efficiency is increased. The proposed charge pump circuit has been simulated using Spectre in the TSMC 0.18 μm CMOS process. The simulation results show that the maximum voltage conversion efficiency of the new 3-stage cross-coupled circuit with an input voltage of 1.5 V is 99.8%. According to the comparison results of the conventional pump and the enhanced charge pump proposed, the output ripple voltage has been significantly reduced.

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1. INTRODUCTION

Using switched-capacitor charges, charge pump circuits have been often used to convert a dc input voltage to another dc output voltage; it can generate a voltage larger than the supply voltage or lower than the ground of the chip. Charge pumps can provide tens or hundreds of mA current for subsequent signal processing blocks. Supplying a stable and higher DC voltage to all the embedded Intellectual Properties (IPs) becomes an important challenge.

Advantages of charge pump circuits are their low cost, low EMI, and small size. For these reasons, the design issues are always focused on high pump-efficiency, high power-efficiency, higher output power, and low output ripple voltage.

In 1976 J. F. Dickson proposed a Dickson charge pump with diode-connected NMOS transistors instead of diodes. This kind of charge pump can be easily implemented in a standard CMOS process [1]. However, due to the body effect, the high NMOS transistor threshold voltage reduces the boost efficiency. J. T. Wu and K. L. Chang proposed dynamic charge transfer switches (CTS) instead of diode-connected NMOS transistors, making the NMOS fully open to eliminate the threshold voltage [2]. However, in multi-stage charge pump circuits, the diode-connected CMOS transistors still exist in the final output stage. This will lead to a certain threshold loss problem, while the substrate effect still exists.

Cross-coupled voltage doublers are widely used, due to its less voltage drop between the drain terminal and source terminal of each switch. The main disadvantage of cross-coupled voltage doublers is that they have three kinds of reversion loss: the reversion loss from the output to the flying capacitors, and the reversion loss from the flying capacitors to the input, the reversion loss from the output to the input [3].

The break-before-make mechanism, the first-level gate-control mechanism, new gate control strategies, the transfer blocking technique and the modified pre-charge scheme are proposed to eliminate the reversion loss in the conventional cross-coupled voltage doubler. However, we need extra level shifters or blocking

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