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Enhanced Static Noise Margin and Increased Stability SRAM Cell with Emerging Device Memristor at 45-nm Technology[1]

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Abstract—Very Large Scale Integrated (VLSI) technology has conquered a momentous transformation and adaption. The glory of achieving these platforms goes to aspect ratio shrinking. Not only the dimensions are scaling down, but the revolution is forcing the designers to switch all circuits from one device level to another emerging devices. In this conflict, memristors are capable of making their roots stronger in VLSI domain as compared to other emerging devices. In this paper it is presented the research of static noise margin, highlighting the new fidelity issue i.e. the noise that has great impact on retention voltage of SRAM cell and this effect in memristive cell is less as compared to conventional 7T SRAM cell. Simulations and results have been performed and obtained from 7T SRAM and memristive 7T SRAM cell at 45 nm technology. In this paper, impact of the cell and pull-up ratio with their comparisons is also discussed.

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1. INTRODUCTION

Complementary Metal Oxide Semiconductor (CMOS technology) is facing dreadful challenges at channel length below 45 nm. These challenges are surfacing as sub-threshold leakage current, hot carrier effects, device mismatch and carrier mobility degradation. In conflict to this multiple gate transistor conquered these bulk CMOS issues. It is luminous that forthcoming technology materials should display higher stability, mobility, scalability and reduced short channel effects with respect to process variations.

Memristor is very promising device in minds of designers as it comprises of most desired features. It is compact, consumes less area, low power and low leakage. In addition to these advantages, it also makes system non-volatile as memristor has non-volatile nature i.e. it is able to retain data even when power supply is removed. There is a great demand to search the potential of rising technology by designing circuits with memristors (Fig. 1) and comparing their performance with existing technologies i.e. CMOS technology.

A physical memristor consists of two platinum electrodes, and the resistance of this device depends on the polarity, magnitude and length. When the voltage is turned off, the resistance remains as it did just before it was turned off. This makes the memristor a nonvolatile memory device.

In Fig. 2 two terminal memristor utilize titanium dioxide as the resistive material. In other memristors, silicon dioxide material can be used. However, titanium dioxide works better. When a voltage is applied across the two terminals, as shown above, the oxygen atoms in the material disperse towards left or right. And then, the material will become thinner or thicker depending on the polarity of the voltage, thus causing a change in the resistance. All the parameters of transistor and memristor are calculated with the help of Cadence tool at 45 nm technology.

Due to contentious scaling in memory device dimensions, supply voltages and process variations put cardinal challenges to forthcoming memory designs and high performance of circuits [1–3]. Currently, it has been proposed to replace CMOS based devices in SRAM with memristors based SRAMs. These memristive

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