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Analyzing the Impact of Augmented Transistor NMOS Configuration on Parameters of 4x1 Multiplexer

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Abstract—This paper represents the power and delay analysis of 4×1 multiplexer based on Augmented Transistor NMOS (AT-NMOS) configurations. Transistor's total channel width at multiple levels are considered to determine the leakage power and delay performance at 45 nm technology. It is evaluated that the performance parameter is improved in the proposed design based on Augmented Shorted Gate-Source PMOS with NMOS (ASG-S PMOS-NMOS) configuration as compared to the 4×1 multiplexer based on Static Threshold AT-NMOS (ST-ATNMOS) configuration. Using this combination, we obtain the desired performance parameters of the design. In this paper, two types of 4×1 multiplexer models are introduced. It is shown that the leakage power can be largely reduced. The delay performance is also improved up to 5% at 1 V power supply under consideration of multiple levels of transistor's channel width due to evaluation of different AT-NMOS configurations based 4×1 multiplexer models. The simulation work has been carried out using the Cadence Analog Virtuoso Spectre Simulator at 45 nm CMOS technology.

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1. INTRODUCTION

Minimization of power dissipation is becoming a main motive for VLSI engineers. This paper shows an efficient power model for the system, which contains a low leakage power dissipation. To reduce power, it is most necessary to explain new types of circuits in order to find better design techniques [1].

Here for achieving this target, two types of model of 4×1 multiplexer are proposed. These two types of 4×1 multiplexer are based on two different types of MOS configuration. These two different configurations follow the principle of body effect [2].

The body effect over the channel can be explained using a variation of the threshold voltage described by the following equation:

$$V_{\text{TB-NMOS}} = V_{\text{T0}} + \gamma_n \left[\sqrt{V_{\text{SB}} + 2\varphi_{\text{B}}} - \sqrt{2\varphi_{\text{B}}} \right], \quad (1)$$

where $V_{\text{TB-NMOS}}$ is the threshold voltage with substrate bias for *n*-channel MOS, and V_{T0} is the zero-V_{SB} value of threshold voltage, γ_n is the body effect parameter for *n*-channel MOS, and $2\varphi_{\text{B}}$ is the estimated potential drop between surface and bulk across the depletion layer when $V_{\text{SB}} = 0$ and gate bias is enough to assure the presence of channel. Equation (1) describes a reverse bias ($V_{\text{SB}} > 0$) which affects a raise in threshold voltage V_{TB}; it requires a larger gate voltage before the channel settles.

According to the above mathematical expression, if the physical parameter $2\varphi_{\text{B}}$ is assumed to be constant, the threshold voltage is directly proportional to the source-to-bulk potential. The physical parameter depends on the transistor's physical dimensions. The body effect parameter is also known as fabrication process parameter.

Body effect parameter γ_n can be evaluated by formula:

$$\gamma_n = (\sqrt{2q\varepsilon_{\text{sil}} N_A}) / C_{\text{ox}}, \quad (2)$$

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