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Output Buffer for +3.3 V Applications in a 180 nm +1.8 V CMOS Technology

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Abstract—A new output buffer realized with low-voltage (+1.8 V) devices to drive high voltage signals for +3.3 V interface, such as peripheral component interconnect extended (PCI-X) applications in a 180 nm CMOS process is proposed in this paper. As PCI-X is a +3.3 V interface, the high voltage gate–oxide stress poses a serious problem to design PCI-X I/O circuits in a 180 nm CMOS process. The performance of the proposed output buffer is examined using Cadence software and the model parameters of a 180 nm CMOS process. The experimental results have hither to confirm that the proposed output buffer can be successfully operated at 100 MHz frequency without suffering high voltage gate–oxide overstress in the +3.3 V interface. A new level converter realized with +1.8 V devices that can convert 0/1 V voltage swing to 0/3.3 V voltage swing is also presented in this paper. The simulation results have confirmed that the proposed level converter can be operated accurately without any voltage drop. The topology, however, reports low sensitivity and has features suitable for VLSI implementation. The proposed circuits are suited for low power design without performance degradation.

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1. INTRODUCTION

At present semiconductor device market demands manufacture of storage devices having higher operating potentiality, and this triggers another surge in the switching speed. The power consumption has become a major issue on portable electronic systems.

As a result, the level converter should have enough current to meet the requirements of transmission speed. This shows considerable current fluctuations during a short span of time (di/dt), which may raise the switching noise on the power supply lines. In case of large capacitive loads, non-negligible voltage bumps are observed on the power supply lines. These are mainly due to the inductive bond wires, package and board traces, which may result in power supply and ground–bounce (switching noise or Ldi/dt noise). This noise can also lead to data transition delay, oscillation at the end of signal transitions and cross-talk between adjacent signal lines. Moreover, it can even cause malfunctioning of the circuits that are connected to the same supply lines [1].

In order to decrease the core power supply voltage V_{DD} the thickness of the gate oxide in the semiconductor process has been scaled down. However, the board voltage V_{CC} is still kept at +3.3 or +5 V, such as PCI-X interface. Therefore, the high-voltage stress across the thin gate oxide has become a serious problem in deep submicron (DSM) processes [2]. The I/O circuit must he designed carefully to avoid the high-voltage gate–oxide stress in the mixed-voltage interface [3–9].

The remaining sections of the paper are organized as follows. The conventional level converters are presented in section 2. The new proposed level converter, output buffer and circuit description are presented in section 3 and 4. Simulation results and details of comparative conventional circuits are considered in section 5. Finally, the conclusion is drawn in section 6.

2. CONVENTIONAL LEVEL CONVERTERS

Figure 1 shows the conventional mixed-voltage tri-state output buffer, where transistors P_1 and N_1 are the I/O high-voltage (V_{CC}) devices. The voltage swing of signals IN, EN, and ENB is from GND to V_{DD}, but the voltage swing of the output signal is from GND to V_{CC}. If the board voltage V_{CC} is equal to V_{DDH}, the output stage (P_1 and N_1) can be operated without suffering high-voltage gate–oxide stress. In Fig. 1, the level

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