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Efficiency Analysis of Techniques for Weighting Elements Arrangement on the Chip of Unary Digital-to-Analog Converter

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Abstract—The paper presents a review of realizations of the matrices of unary DAC weighting elements. A mathematical model of unary DAC taking into account the systematic error has been built. The static characteristics were simulated, and conclusions were made regarding the preferred techniques of forming the matrix of weighting elements for reducing the nonlinearity of unary DACs.

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1. INTRODUCTION

Digital-to-analog converter (DAC) is a device for transforming a digital code, usually binary, into analog signal in the form of current or voltage proportional to the digital code value. Parallel DACs have the highest acceptance in telecommunication systems. Among the parallel DAC architectures, we can separate the three main ones: binary, unary and segmental [1, 2].

The binary architecture performs the summation/division of binary-weighted values. The number of such values is equal to the number of bits N of DAC. The control of elements is performed directly by bits of input binary code. The unary architecture performs the summation/division of equally weighted values. The weighting elements in this architecture, the number of which is equal to $2^N - 1$, have the same nominal. The control of elements is performed by the unary code, the formation of which requires the use of thermometric decoder [3]. The segmental architecture combines both architectures described above.

The main parameters of DAC include differential nonlinearity (DNL) and integral nonlinearity (INL). The manufacturing tolerance causing mismatch of values of weighting elements is one of the main causes of static nonlinearity of DAC. The use of unary architecture makes it possible to compensate the systematic component mismatch of values of weighting elements by an appropriate (hereinafter compensating) arrangement of weighting elements in the chip layout and, consequently, to reduce the static nonlinearity of DAC.

The compensating arrangement of weighting elements makes it possible to reduce the impact of systematic error and decrease the DAC nonlinearity without any additional manufacturing operations, such as postproduction adjustment or calibration of the integral circuit. An array of weighting elements located on the chip is called matrix of weighting elements. Note that since the binary architecture can be realized on elements with equal nominals, the systematic error compensating technique using the compensating arrangement of elements in matrix can be extended to all architectures of parallel DACs.

Different techniques of arrangement of weighting elements exist that differ in terms of the realization complexity and the efficiency of reducing the static nonlinearity of DAC. The arrangement techniques of weighting elements are classified by the method of systematic error compensation: with symmetric and asymmetric arrangement of elements, and by the method of weighting element formation: with and without division into parts. Table 1 presents the publications describing the techniques [4–11] corresponding to the above division into groups.

Among the specified techniques, two most common techniques can be singled out: the Lee-Lin-Kuo technique from the group of techniques with asymmetric arrangement and without division of element into parts [8] and the Palmers-Wu-Steyaert technique from the group of techniques with symmetric arrangement

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