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Designs of Multi-bit Sigma Delta Modulator

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Abstract—This paper presents new design variants of third order multi-bit sigma delta modulator (SDM): low distortion SDM and cascaded SDM. The proposed modulator based on the conventional SDM such L-0 MASH (Multi-stAge noise SHaping) and interstage feedback topology. The MASH SDM is not a single loop system. One of the drawback is that performance is limited by uncancelled noise from the first modulator and interstage feedback topology only cancels nonlinear errors introducing by multi-bit DAC in the final stage, but the rest stage still contains DAC nonlinearity errors without any noise shaping which still degrade overall system performance. An improved version of cascaded multi-bit SDM is proposed to overcome these problems mentioned above. In addition a third order low distortion SDM is also proposed. Simulation results verify the superiority of the both proposed modulator.

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1. INTRODUCTION

Delta sigma analog-to-digital converters (ADC) which are based on oversampling and noise shaping are suitable candidate for high resolution of relatively narrow to medium bandwidth signals.

In order to achieve high resolution in an oversampled ADC, either the sampling frequency should be increased or the modulator should provide more efficient noise shaping. The former results in increased power consumption whereas the latter might result in instability. On the other hand it is possible to increase the number of quantizer bits which in turn will reduce the number of quantization levels that will reduce both the in band and out of band quantization noise power, resulting in improved signal to noise ratio (SNR) and improved stability, enabling also the possibility to reduce oversampling ratio requirement [1]. A notable disadvantage of multi-bit system is necessity to achieve excellent integral linearity.

In single loop sigma delta modulator (SDM), the error due to multi-bit digital-to-analog converter (DAC) nonlinearity effectively enters the modulator at its input. Therefore, the modulator's linearity and resolution are limited by the precision of the multi-bit DAC. Therefore achieving high integral linearity and low total harmonic distortion (THD) appears to require precisely matched components [2].

Different strategy, which relies on cancellation rather than filtering of the quantization noise, is to use a multistage structure for the modulator. It consists of cascade of several lower order single loop modulators, each with its own quantizer. Each single loop modulator in the cascade converts the quantization error from the proceeding modulator. The input to the second and ensuing stage of the cascaded structure are the quantization error from the previous stages [3]. One of the advantages of cascaded modulator is that it can be made stable, if the modulators it is composed of are stable. Cascade architecture also cancels or noise shaped the nonlinearity errors induced by multi-bit DAC in each stage [4].

This paper features:

— Design of 3rd order cascaded multi-bit modulator because multi-bit modulator are particularly attractive for achieving high dynamic range.

— This work focus on the noise shaping of the nonlinearity errors of multi-bit DAC using interstage feedback path such that to certain extent it relax the constraints on the design of multi-bit DAC.

— Proposed design of 3rd order low distortion SDM to overcome the problem of harmonic distortion.