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Implementation of Complex Digital PLL for Phase Detection in Software Defined Radar

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Abstract—Software defined radar (SDR) has been the latest trend in developing enhanced radar signal processing techniques for state-of-the-art radar systems. SDR provides tremendous flexibility in reconfigurable design and rapid prototyping capabilities on FPGA platform. To cater real-time processing for high-speed radar, COordinate Rotation Digital Computer (CORDIC) unit has been utilized as a core processing element in a complex digital phase locked loop (DPLL) for digital demodulation of received signal. Since the real-time systems are required to handle extremely high sampling rates, the pipelined architecture of CORDIC processing element has been chosen for its inherent high system throughput. The architecture is optimized in terms of bit-length for better convergence and loop performance of the first order complex DPLL during demodulation. The BOXCAR filter has been used as a low pass filter in the output stage of the detector for better information recovery from narrow samples with little energy signal without incurring hardware overhead. Extensive MATLAB simulations have been added to show the effectiveness of the design for the application of radar phase detection.

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1. INTRODUCTION

Software defined radar (SDR) is the most versatile system where the majority of hardware processing is replaced by software with great precision. SDR has the unique capability to retrieve high precision information concerning the velocity of moving object, the distance and the direction [1, 2]. Phase detection in radar receiver is a vital and sensitive process in real-time target detection.

Voltage controlled oscillator (VCO) is used in a large number of radio communication systems including radar systems. But inherent nonlinearity and the lack of spectral purity in such oscillator makes the phase detection process difficult for obtaining the output signal spectrally pure over the desired range of frequencies [3, 4]. Modulators/demodulators based on direct digital frequency synthesizers (DDFS) are widely accepted in the radar or communication industry due to their superior performance [5].

Quantization noise is another unavoidable byproduct of digital systems. Quantization error creates an undesired noise which remains impregnated over the demodulated signal. Efforts have been made to design a quantization-error-free digital phase detector using an optimized architecture of pipelined COordinate Rotation Digital Computer (CORDIC) and implement it on a high-speed digital reconfigurable FPGA platform. In this paper, we have proposed a first order complex digital phase locked loop (DPLL) for better switching speed, frequency resolution and lower phase noise as compared to the classical radar phase detector.

The flexibility, modular design and multiplierless architecture of CORDIC make an urge for the inclusion of SDR in phase detection. The iterative formulation of CORDIC algorithm was first developed by Jack E. Volder in 1959 [6] for the multiplication, division and computation of trigonometric functions, such as sine, cosine, magnitude and phase with great precision. The CORDIC algorithm can be implemented by using simple shift and add functions. These functions can be implemented by using complex multipliers, variable shift registers or multiply accumulator (MAC) units. Considering high throughput, reduced complexity and easier reconfigurable design of CORDIC, it can be highly suitable for low cost hardware solutions on FPGA platform [7, 8].

Nowadays smaller mobile radars are being used on modern automotive vehicles as an anti-collision device. Some ultralight mobile radars are also being used to monitor hostile targets by military forces.