ISSN 0735-2727, Radioelectronics and Communications Systems, 2016, Vol. 59, No. 3, pp. 109–116. © Allerton Press, Inc., 2016.
Original Russian Text © T. Varshney, S. Khandelwal, S. Akashe, 2016, published in Izv. Vyssh. Uchebn. Zaved., Radioelektron., 2016, Vol. 59, No. 3, pp. 18–29.

Development of 3T eDRAM Gain Cells for Enhancing Read Margin and Data Retention[1]

Tarushree Varshney*, Saurabh Khandelwal, and Shyam Akashe
ITM University, Gwalior, India
**e-mail: tarushree.varshney@gmail.com*
Received in final form April 1, 2015

Abstract—This paper presents three transistors (3T) based Dynamic Random Access Memory (DRAM) cell in which noise, static power, and data retention voltage (DRV) have been reduced. The spesified parameters in the proposed eDRAM gain cell were improved by connecting the source of storage device to the read word line signal instead of supply voltage. As we all know, power consumption plays a vital role in VLSI design and thus, it is enumerated among the top challenges for the semiconductor chip industries. With the intention to maintain the performance of write operation, we diminish DRV and increase the read margin of eDRAM cell with our designed circuit which is introduced as "A Boosted 3T eDRAM gain cell". It is a kind of eDRAM cell that utilizes a read word line (RWL) via three PMOS transistors instead of NMOS transistors. PMOS devices are preferred as they have radically less gate leakage current, which confer better results for data retention and thus, boost up the read margin of the cell. Simulation results have been obtained by using Cadence Virtuoso Tool at 45 nm technology for the proposed model. Based on simulation results we can conclude that the parameters of the proposed eDRAM gain cell essentially improved as compared with convertional eDRAM gain cell and the achieved parameters are as follows: static power is 0.767 pW, DRV is 142.009 mV and noise is 8.421 nV/Hz$^{1/2}$.

DOI: 10.3103/S073527271603002X

1. INTRODUCTION

Semiconductor memory is one of the most useful VLSI (Very Large Scale Integration) building blocks which is an electronic device to store the data in binary form, and usually used for computer memory [1]. In order to maintain the historical growth in chip performance, designers must continue to deliver memory solutions for achieving low static power and high operating speed.

SRAM (Static Random Access Memory) has been the conventional choice for the implementation of embedded memories due to its high-access speed and refresh-free static data retention. However, in modern systems, it has several drawbacks including its number of transistors, its impeded functionality under voltage scaling, and the aforesaid static leakage currents from the supply voltage V_{DD} to GND.

In recent time, the embedded DRAMs (eDRAMs) have achieved enormous popularity among the members of research community due to their features such as small cell size, small cell leakage, and non-ratioed circuit operation. There have been a number of victorious eDRAM designs based on conventional 1T1C DRAM cells, as well as logic-compatible gain cells [2, 3]. 1T1C cells are denser than gain cells, but at the cost of a capacitor process, and the noise margin is reduced significantly at low voltages as the read operation is based on the charge sharing principle.

The production of gain cells is based on logic strategy that allows them to be built in a standard CMOS process with minimal modification. The cell consists of three transistors, or even two transistors when used with elusive read control circuits, achieving almost 2-fold higher bit cell densities than SRAMs [4, 5]. In addition, gain cells can have smaller cell leakage current than SRAMs in sleep mode due to a small number of devices and super cut-off biasing condition. The write margin is superior in comparison to SRAMs since there is no controversy between the access device and cross-coupled latch in an eDRAM cell. In this work

[1] This paper was supported by ITM (Gwalior) with the collaboration of Cadence System Design (Bangalore, India).