ISSN 0735-2727, Radioelectronics and Communications Systems, 2016, Vol. 59, No. 2, pp. 66–73. © Allerton Press, Inc., 2016.
Original Russian Text © V.I. Timofeyev, E.V. Semenovskaya, O.M. Falieieva, 2016, published in Izv. Vyssh. Uchebn. Zaved., Radioelektron., 2016, Vol. 59, No. 2, pp. 23–32.

Electrothermal Analysis of GaN Power Submicron Field-Effect Heterotransistors

V. I. Timofeyev*, E. V. Semenovskaya, and O. M. Falieieva*****

National Technical University of Ukraine "Kyiv Polytechnic Institute", Kyiv, Ukraine
**ORCID: 0000-0003-0515-1580*
***ORCID: 0000-0003-2421-4903, e-mail: semprih@gmail.com*
****ORCID: 0000-0002-0977-6900*

Received in final form October 21, 2015

Abstract—Physical processes and self-heating factors of in a power submicron field-effect heterotransistor have been considered. Mathematical models were proposed and the electrothermal analysis of heterotransistor parameters and characteristics was performed. The impact of thermal processes on parameters of the circuit model and the output frequency characteristics of submicron heterotransistor was shown on the basis of analysis of temperature fields. The relationship of the transistor thermal resistance as a function of its geometry and thermophysical parameters has been established.

DOI: 10.3103/S0735272716020035

1. INTRODUCTION

At present the heterostructure electronics based on materials with A^3B^5 structure occupies dominant position in systems of data processing and transmission as compared to silicon VLSI circuits. In particular GaN VLSI has gained widespread use. Such application of the specified material is determined by its technical properties making it possible to obtain high-speed and high-power components of the millimeter wave solid-state electronics. The application of materials based on gallium nitride (GaN) in case of reducing the active region of transistor heterostructure to submicron size makes it possible to attain a high speed of electron transit in devices and minimize dissipative losses. As a result, the heterostructure technology enables us to develop high-speed and high-frequency solid-state devices for low-noise and power gain devices.

These structures, generally, have the gate length of several tenths of micrometer that in the case of high-power structures results in a maximum release of power in the region of strong electric fields under the gate and near the drain edge of heterotransistor gate. Such localization of thermal fields materially affects the electrophysical and field-speed characteristics due to the self-heating effect. This self-heating can be limited at the expense of proper selection of design, materials of heat sinks and the package with appropriate values of thermal resistances. Due to the effects of strong field under the gate and the local heating of electron gas to temperatures as high as several thousands of Kelvins, the overheating of structure increases. This rise of temperature cannot be eliminated by design methods.

Thus, the description of self-heating in real transistor structures for determination of their electrothermal behavior is related to both the simulation of thermal fields and description of processes in the region of strong field, where overheating is most pronounced. Variation of electron gas parameters due to the rise of temperature leads to the appearance of high local gradients of temperature which affect both the electric characteristics of the transistor structure and parameters of transistor reliability.

At present, besides the technological means of heat removal, a particular attention is paid to taking into account and correcting the impact of thermal effects on electric parameters at the design stage of the specified devices. This primarily concerns the development of adequate mathematical models of electronic devices with due regard for the impact of self-heating effects.