Load Network for Microwave Class F Amplifier

A. Yefymovych^{1*}, V. G. Krizhanovski¹, V. Kovalenko¹, R. Giofrè², P. Colantonio², R. Danieli² ¹Donetsk National University, Donetsk, Ukraine ²University of Rome Tor Vergata, Rome, Italy *e-mail: vefymovych@gmail.com Received in final form April 17, 2015

Abstract—In this paper we present the technique for development and calculation of the load network for the microwave class F power amplifier (PA) with addition of the third and the fifth voltage harmonics. The suggested load network compensates negative influence of parasitic elements of the transistor (of output capacitance and of output inductance) on the operation of class F PA. Also the load network allows one to decrease the negative influence of some real properties of the supply circuit shunt capacitor and the blocking capacitor on the impedances, which are created by the load network at the transistor chip. We have obtained the calculation formula for the transistor load resistance at the specified output power for class F PA with addition of the third and the fifth voltage harmonics.

DOI: 10.3103/S0735272715070018

INTRODUCTION

During the development of class F transistor power amplifiers (PA), which operate in microwave band, there occurs the need for the account of real properties of the transistor and load networks, that in practice reduce the efficiency of an amplifier [1-4]. For class F PA it is an important problem to take into account such parasitic elements of the transistor as the output capacitance C_{out} and output inductance L_{out} [5–11]. These elements form the *LC* circuit, which does not allow the load network to create impedances on transistor chip (parallel to C_{out}), that are required theoretically [12].

In [6] the author has suggested a technique for the compensation of C_{out} and L_{out} for class F PA with the addition of the third voltage harmonic. According to [12] theoretically such an amplifier provides drain efficiency $\eta_d = 90.69\%$ under the condition that impedances for all even harmonics are equal to zero at the transistor chip. In practice, the value $\eta_d = 90.69\%$ is unattainable, because there exists knee voltage of the transistor V_{knee} , which principally limits the efficiency of an amplifier. In [12] it is shown that the addition of a supplementary fifth voltage harmonic increases η_d by 4.08%.

In [5] the authors have proposed the approach, which allows one to synthesize the load network based on the lumped elements, that provides the compensation of negative influence of C_{out} and L_{out} up to the *n*th harmonic. However, in [5] it has been established that to control more than five harmonics is rather difficult, because in the microwave band one cannot obtain required impedance at all harmonics above the fifth one due to design constraints and manufacturing accuracy of the load network. In addition, the utilization of harmonics above the fifth one does not lead to significant increase in the efficiency of the amplifier [5, 12].

Practical implementation of a load network, which is proposed in [5], in the microwave band can cause difficulties connected with the physical realizability of a network at the stage of substitution of lumped elements by transmission lines with distributed parameters. This circuit allows one to obtain the impedances on the chip of the transistor, which are equal to zero for even harmonics and which are equal to infinity for odd harmonics under the condition that in one of the circuit sections the impedance for the higher even and odd harmonics is equal to zero. In practice, this requires the use of additional printed circuit board, which is connected by a conductor to the main board [5], that makes the production of a network more complicated. Also in [5] there are no relations, which enable one to calculate the parameters of the load network based on the required load impedance of the transistor for the first harmonic $Z(f_0)$ (required output power), for the specified load resistance R_{ld} . In [5] the authors have performed only the optimization of $Z(f_0)$ in order to obtain the maximal power-added efficiency (PAE).

In this paper we propose the technique for development of the load network for the microwave class F PA with addition of the third and the fifth voltage harmonics, which allows one to compensate the negative