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Inter-Modulation Linearity Investigation of an Optimally Designed and Optimally Biased LNA for Wireless LAN

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Abstract—This paper presents the effects of process parameters variations of new underlap SOI MOSFETs (underlap SOI technology with spacer covered) on linearity investigation of cascode low noise amplifier (LNA) for wireless LAN application. By quantifying the linearity of the LNA in-terms of third order intercept (IP3), the paper presents guidelines for optimum value of spacer s, film thickness T_{Si} doping gradient d and gate length L_G of the underlap device for linearity enhancement of the LNA. Based on a new Figure-of-Merit of LNA (FoM_{LNA}) involving available signal power gain G, IP3, noise figure (NF) and dc power consumption P_{dc}, it has been found that FoM_{LNA} in double gate (DG) configuration is much higher than single gate (SG) one at the optimum gate overdrive V_{OD} = 75 mV. This is due to a combined effect of higher value of G and IP3 in the DG configuration. By comparing with limited available experimental data of 0.18 μm bulk technology, it has been found that using new underlap SOI MOSFETs with gate length of L_G = 60 nm (effective gate length L_{eff} = 92 nm) optimally designed and optimally biased LNA gives almost two times improvement in the proposed FoM_{LNA}. With optimal bias the LNA achieved the following indicators: NF ~ 2.27 dB, IP3 ~ +7.75 dBm, G ~ 20.86 dB and power consumption equal to 2.5 mW.

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1. INTRODUCTION

Today the wireless handset market is characterized as one of the largest global markets for the radio frequency (RF) semiconductor industry [1]. Portable wireless computing devices have fuelled the demand for local area networks (LANs) [1]. More recent among them is orthogonal frequency division multiplex (OFDM) based wireless LAN which provides high data bit rate in the 5–6 GHz ISM band [2].

In this band for designing a front-end LNA block different solutions have been proposed designed and fabricated by using bipolar technologies such as GaAs HBT (Lott 1996), MESFET (Kobayashi 1995) and SiGe bipolar technology (Soyuer et al. 1997), but they face integration problem with base band section, consume much power and have higher cost as compared to SOI–CMOS technology. Therefore, this paper considers a more cost-effective, less power consuming and compatible in integration with base band section solution for LNA realization based on Silicon-on-Insulator (SOI) MOSFETs. As a result of proper engineering of SOI–MOS device, it has been found that the drain and source capacitances with respect to the body are significantly reduced [3]. Furthermore, SOI gives inherent suppression of short-channel effect (SCE) as well as an improved lateral isolation compared to bulk technology [3, 4].

The advanced down-scaling of MOS technology enables us to design low noise, high gain amplifiers with low power consumption for GHz application. Many trade-offs involved in designing LNA included noise figure (NF), linearity, gain, impedance matching, and power dissipation. However, the linearity of MOSFETs is getting worse as the process scales down [5], which has motivated the development of several linearization techniques.

Due to possible large interference signal tones at the receiver end along with the carrier, the LNA is expected to provide high linearity, thus preventing the inter-modulation tones created by the interference signal from corrupting the carrier signal; therefore, the linearity study is highly essential in establishing the LNA suitability for realizing the emerging wireless systems.