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Modelling and Simulation of FinFET Circuits with Predictive Technology Models[1]

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Abstract—During analysis of complexities of the Metal Oxide Semiconductor Field Effect Transistors (MOSFET) technology to obtain the adequate gate control above the channel, FinFET technology founded on Double or Multiple gate (more than two gates) arrangement is improved technology alternative for auxiliary lessening the size of the MOSFET. In favor of double or dual gate MOSFET (DG MOSFET) the gate control above the channel that formed in between source and drain terminal efficiently. As a result the numerous short channel effects like sub-threshold swing, Drain Induced Barrier Lowering (DIBL-effect), gate leakage current, punch through etc. do not include growing of carrier concentration addicted to the channel. This paper is devoted to specific explanation on the subject of the DG MOSFET composition with its exacting kind termed the same as FinFET technology. FinFET technology has four modes such as shorted-gate (SG) mode, low power (LP) mode, independent-gate (IG) mode and hybrid IG/LP mode and performed the comparative analysis of stand-by leakage (when the circuit is idle), delay, total power consumption and noise of the circuit, using Cadence Virtuoso tool at 45 nm.

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1. INTRODUCTION

As we reduce auxiliary the size of the MOSFET technology numerous short channel effects (SCE) are shaped. So as an alternative of MOSFET technology DG MOSFET technology based on double or multiple (more than two) gate devices include superior control above the short channel effects. Above all the FinFET technology gives advanced scalability limits of the DG MOSFET compared to the MOSFET. It gives recovered performance compared to the bulk Silicom-CMOS technology.

FinFETs are seen to be tough applicant for substituting the bulk or planar Silicon-CMOS technology from 60 nm beyond. Several unusual ICs like DRAM, digital logic, flash memory, SRAM etc. have previously been confirmed. Because of its enhanced scheming above sub-threshold leakage current, FinFETs are rewarded for the elevated gain analog purposes and get enhanced effect in the RF applications [1].

The multi-gate or more than two gate MOSFETs are recommend to be made dissimilar for concurrently repressing the sub-threshold leakage and gate dielectric leakage currents in the sub-45-nm CMOS technologies. Two electrically coupled gates and thin silicon body repress the SCE in a double-gate MOSFET, reducing sub-threshold leakage current [4]. Improved gate control above the channel (lower sub-threshold leakage or swing) and suppressed SCE allow to use of thicker gate oxide in a double-gate MOSFET as evaluated to a bulk single-gate transistor. The gate-oxide leakage current of a double-gate transistor is thus considerably condensed.

The FinFET is the large amount effective option along with the DG MOSFET architectures due to the self-alignment of two gates, it is submitted to as a quasi-planar device, since its geometry is in vertical direction (the fin height). The narrow fin structure arranged efficiently by spacer fin patterning flexibly

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