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Analysis and Design of Low Power SRAM Cell Using Independent Gate FinFET[1]

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Abstract—Scaling of bulk MOSFET faces great challenges in nanoscale integration technology by producing short channel effect which leads to increased leakage. FinFET has become the most promising substitute to bulk CMOS technology because of reducing short channel effect. Dual-gate FinFET can be designed either by shorting gates on either side for better performance or both gates can be controlled independently to reduce the leakage and hence power consumption. A six transistor SRAM cell based on independent-gate FinFET technology is described in this paper for simultaneously reducing the active and standby mode power consumption. A work is focused on the independent gate FinFET technology as this mode provides less power consumption, less area consumption and low delay as compared to other modes. Leakage current and power consumption in independent gate FinFET is compared with tied gate or shorted gate FinFET SRAM cell. Moreover, delay has been estimated in presented SRAM cells. Further, leakage reduction technique is applied to independent gate FinFET 6T SRAM cell.

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INTRODUCTION

The scaling of bulk CMOS has lead to improvement in performance of digital circuits however faces significant challenges due to process technology limits. Obstacles of scaling to sub-45nm gate lengths include short channel effects (SCE), sub-threshold leakage, gate dielectric leakage and device-to-device variations [1].

As the channel length of a conventional MOSFET is reduced, the drain potential begins to strongly influence the channel potential, thereby causing sub-threshold leakage. Furthermore, as the gate dielectric thickness is reduced to assert stronger control over the channel area, the gate tunneling leakage current increases significantly. Further scaling of the gate insulator thickness causes an unreasonable increase in the power consumption due to the gate leakage [2].

In general, SCE arises from several geometrical effects in which the channel length becomes equal to the depletion layer. Drain Induced Barrier Lowering (DIBL) is the major effect produced by SCE, in which high electric fields from the drain can lower that barrier that is supposedly only controlled by the gate. This effect can degrade the devices sub-threshold slope and cause changes in the threshold voltage (V_{th}).

In order to increase the gate control of the source-to-channel barrier, gate dielectrics must be made thinner. Thinner gate dielectrics allow more tunnel current to pass between the gate electrode and the body of the device. This gate current results in excess power dissipation.

Several materials have been used to reduce SCE, such as high-K gate dielectrics. These materials, such as HfO_2 and ZrO_2, may provide increased gate capacitance with thicker films that provide a larger tunneling barrier, and therefore lower gate leakage current. But many integration challenges have prevented their use in high performance Silicon based technologies [3].

As we go down below 65nm technology, there seems to be no viable options of continuing forth with the conventional MOSFET. Therefore, multi-gate FETs such as planar double gate FETs and FinFETs have been proposed for low power digital CMOS technologies to reduce SCE.

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