ISSN 0735-2727, Radioelectronics and Communications Systems, 2010, Vol. 53, No. 7, pp. 356–366. © Allerton Press, Inc., 2010.
Original Russian Text © S. Borisov, A.S. Korotkov, 2010, published in Izv. Vyssh. Uchebn. Zaved., Radioelektron., 2010, Vol. 53, No. 7, pp. 21–30.

Procedure for Building a MOS Transistor High Frequency Small-Signal Model

S. Borisov and A. S. Korotkov

Saint Petersburg State Polytechnical University, St.Petersburg, Russia

Received in final form January 28, 2010

Abstract—This paper examines a procedure for building a MOS transistor small-signal equivalent circuit for the high frequency range. Procedures are proposed for determining the ac and dc parameters. The simulation results and experimental data are also presented.

DOI: 10.3103/S0735272710070034

1. INTRODUCTION

The silicon CMOS process is now dominant making it possible to create microchips for digital and analog devices in a wide frequency range. The microchip designing is performed by using the computer simulation technique based on models of electronic components, first of all, MOS transistors. The building of such model implies that MOS transistor is conventionally divided into two regions: "internal" and "external". The physical processes occurring in the "internal" region are determined by the properties of channel. The physical processes taking place in the "external" region are determined by the impact of the substrate and also by the technological and design peculiarities of transistor. The impact of "external" region causes the appearance of additional parasitic elements that cannot be neglected during the design process [1–4]. Figure 1 presents the physical structure of MOS transistor marking out the elements of MOS transistor equivalent circuit. The "internal" region is represented by equivalent resistance of the channel R_{ds}. The "external" region is represented by the following set of parasitic elements shown in this figure: gate resistance R_g, source resistance R_s, drain resistance R_d, capacitance of the gate-source overlap C_{gs}^{ov}, capacitance of the gate-drain overlap C_{gd}^{ov}, capacitance of the gate-substrate (bulk) overlap C_{gb}^{ov}, parasitic interelectrode capacitance C_{sd}^{par}, capacitances C_{bs}^{p-n} and C_{bd}^{p-n} determined by p–n junctions "substrate–source" and "substrate–drain", respectively, resistances R_{bs}, R_{bd}, and R_{sdb} determined by the properties of the substrate as a distributed parameter conductor. Leads "G", "D", "S", and "B" correspond to the electrode contacts of gate, drain, source, and substrate, respectively.

The known models of MOS transistors, initially developed for digital and low-frequency analog applications, are intended for describing the "internal" region, i.e., for computing the charge distribution in channel, drain current, the transfer and output admittances. The analysis of papers [1–4] shows that MOS transistor model in the high frequency range should take into account the following points: parasitic interelectrode capacitances, the so-called "nonquasi-static" effect describing the behavior of MOS transistor channel as a distributed parameter conductor, the effect of influence of the gate region as a distributed parameter conductor, resistances of the source and drain electrodes; and the effect of influence of the substrate region as a distributed parameter conductor. Thus, the simulation of microchips in the high frequency range involves the need of making a generalized equivalent circuit of MOS transistor with due regard for the listed requirements on the basis of one of the known models of "internal" region, to electrodes of which the parasitic "external" elements are connected. Such circuit is capable of describing the parameters of MOS transistors in the frequency range up to 10 GHz [1, 2]. The designing of line devices involves the use of the model in the form of a MOS transistor small-signal equivalent circuit formed by the linearization of the generalized equivalent circuit.

This paper proposes a procedure for building a MOS transistor small-signal equivalent circuit for the high frequency range with due regard for the impact of both the "internal" and "external" regions. The present paper has the following structure: after a short introduction Section 2 deals with the procedure for building a small-signal equivalent circuit of MOS transistor based on the proposed generalized equivalent circuit; the