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Algorithms of Coding the Internal States of Finite-State Machine Focused on the Reduced Power Consumption

T. Grzes, V. V. Salauyou, and I. R. Bulatava
Bialystok University of Technology, Bialystok, Poland
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Abstract—New algorithms of coding the internal states of finite-state machine (FSM) have been (were) proposed. These algorithms make it possible to reduce the power consumption of sequential devices at the stage of their designing. The algorithms presented are based on solving the minimization problem of the switching activity of FSM memory elements that directly results in the reduced power consumption. The sequential and iterative algorithms of coding the FSM internal states have been proposed that are focused on the input power reduction. The experimental studies corroborated a substantial reduction of the power consumption in devices designed with the use of the described algorithms of coding as compared with the known approaches.

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1. INTRODUCTION

The realization of sequential devices built on Programmable Logic Devices (PLD) involves the coding of internal states that is one of the most important stages in the process of logical synthesis of finite-state machines. The development of special coding algorithms makes it possible both to improve the use of features of the PLD structure and to reduce the power consumption of device that is of paramount importance in designing the mobile devices with battery supply.

The majority of known techniques for determining the value of FSM input power usually neglect the power consumed by the combinatorial circuit and take into account only the power dissipated by memory flip-flops. This is explained by the fact that the power dissipated by flip-flops is much more than the power consumed by the FSM combinatorial circuit. In addition, the power dissipated by the PLD combinatorial circuit is always constant. That is why the main technique of reducing the power consumption in implementing FSM built on PLD implies the need of reducing the quantity of switching of FSM memory elements.

Power P_a consumed by logic element a can be calculated by the following equation:

$$P_a = \frac{1}{2} V^2 f N_a C_a, \tag{1}$$

where V is the supply voltage; f is the maximum operation frequency (maximum frequency used for computation of values of the input and output signals); C_a is the output capacitance of element a; N_a is the switching activity (the average number of changes of the output state during one time cycle of the clock signal) of element a.

All parameters in the right side of Eq. (1), except N_a, are constant values depending on the integrated-circuit process technology. In this context the problem of lowering the device power consumption can be reduced to the problem of minimization of switching activity N_a.

The switching activity of sequential devices is directly related to the coding technique of internal states. The FSM transition to new state results in the change of the code stored in FSM memory elements, while each switching of memory flip-flops increases the total power intake. That is why the selection of the coding algorithm to a great extent affects the switching activity of memory elements and, correspondingly, the power consumed by the device.