Optical Reversible Counter

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Received in final form November 13, 2006

Abstract—The optical reversible counter for optical computer is developed. It permits integral implementation.

DOI: 10.3103/S0735272707080109

It is impossible to imagine modern information handling methods without the use of microprocessor technologies. Meanwhile counters as a rule are included in any processor. These counters are program counters, which indicate the executing command, current status storage counters, frequency scaling counters and others [1–3]. The most important counter’s characteristic is its operating speed which for some electronic counters can come up to $5 \times 10^8$ Hz.

The continuous demands for increasing computers’ technical characteristics stipulates the implementation of new information handling methods. Optical computers have the operating speed which is by several orders higher than electronic ones. Thus by experts preliminary estimations the optical computers’ operating speed will make up $10^{12}$ Hz. If the optical computer is built according to Neman’s scheme its processor’s structure presupposes compulsory use of reversible counter. At present sequential accumulating counter’s [4] scheme for optical computer on the basis of amplitude information presentation method is developed. A reversible counter in optical implementation has not been developed yet. That is why the optical counter’s development with reversal opportunity is of great scientific and practical interest. The optical reversible counter can be used in different information transformation and processing devices.

Proposed optical reversible counter forms output optical signals $Q_0 \ldots Q_n$ conforming to counting cells’ CC state on the basis of two optical input signals $I_p$ and $I_m$. Every counting cell has inputs $I_p$ and $I_m$; it also has CC state $Q_i$ and transfer into next rank $P_i$ and $M_i$ availability signals outputs.

The counter cell’s block diagram is presented in Fig. 1. $I_p$ and $I_m$, which are up-counter (+1), and countdown (–1) inputs respectively, memory cell MC and transfer generators GP and GM are shown in the diagram.

The optical reversible counter (Fig. 2) is built on the basis of optical combiners, optically connected waveguides (OCW) [5], delay line and optical Y-splitters, which possess the amplification property.

Information signals $I_p$ and $I_m$ through optical Y-splitters 11, 12 and optical combiner 21 come to the memory cell input. Memory cell consists of optical combiner 23, OCW 41, two optical Y-scatters 14, 15 and delay line, which provides signal delay for a period $t$ equal to the input signal duration. Transfer generators are composed of OCW 42, 44 and Y-splitters 51 and 52 not possessing amplification property.

Let’s examine reversible optical counter’s work assuming the input of three pulses to the up-counter input (+1) and three pulses to the countdown input (–1).

In the initial state all memory cells are in null state. When the pulse comes to $I_m$ input signal $Q_0$ becomes equal to 1. Transfer signal will not arrive to $P_0$ output. When the second pulse comes, signal $Q_0$ will be equal to 0 and transfer signal appears at $P_0$ output. As a result $Q_1$ signal will become equal to 1. The third pulse will determine $Q_0$ as 1. When the first pulse comes to $I_m$ input $Q_0$ signal will become equal to 1. Transfer signal will not arrive to $M_0$ output. When the second pulse comes $Q_0$ signal will become equal to 1 and the transfer signal will arrive to $M_0$ output. As a result $Q_1$ signal becomes equal to 0. The third pulse will set $Q_0$ signal to 0.

In the initial state all output $Q_0 \ldots Q_n$ signals’ intensities are equal to 0. While feeding the signal with 1 conventional units (c.u.) intensity to $I_p$ input, passing through optical Y-splitter 11, optical combiners 21 and 23 comes to OCW’s input 41. As the signal’s intensity is less than 2 c.u. the pulse easily passes to the output and then through optical Y-splitter 15 comes to $Q_0$ output. From the second Y-splitter’s 15 output the pulse comes to the delay line’s 31 input. At the pulse extinction moment at the $I_p$ input signal from the delay line’s