NONSTRUCTURAL OPTIMIZATION OF DEVICES OF SCALE REPRESENTATION OF INFORMATION WITH HIGH DISCRETENESS

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The paper is devoted to synthesis of images displayed on a scale-type indicator, and to design of hardware dealing with the synthesis problem. It is shown that such technical decisions can be optimized in terms of minimum generalized cost by varying the number of buses in the matrix of indicator's elements. Also, it is proved that the minimized discrete-analog device for information display can be built based on a scale, whose electric implementation represents a matrix with its sides' ratio inversely proportional to the ratio between the generalized cost values of control networks for a single bus in each side.

An increase in information loads on human operators of the present-day radar and communications systems places severe constraints on the forms of data representation [1-3]. This has led to wide application of so-called scale (discrete-analog) mapping of messages, permitting to improve ergonomic characteristics of readout devices and to diminish the amount of errors when we read data off of electronic visualization devices [3-5]. The overall number of indicator elements (IE), used in the readout devices, characterizes the information parameters of the channel of interaction with a human operator, and the discreteness of representation of measurement results. From the ergonomic point of view, the information field (IF) consisting of 30 to 150 IE is considered optimal for devices of personal use [6, 7].

Analysis of information models of the scale representation of data, and of the relevant hardware implementations with readout devices including 30 and more elements, has shown that, irrespective of the mapping technique used, the matrix-type electric layout of information field is preferable. Thus we can reduce considerably the number of indicator's inputs and of control signals required, which permits to minimize the stock of technical decisions and assure their reliability [3, 8]. As a result, in synthesis of visual readout with the aid of IE, which comprise a two-coordinate matrix, we employ specific principles of signal shaping by the indicator buses based on activation of certain groups of the readout indices. At the same time, the matrix connection gives no way of arbitrary selection of the elements, and imposes substantial limitations of excitation signals, which depend on IE type [8, 9].

The hardware decision creating a pattern on the information field usually contains some digital structure responsible for synthesis of logic signals to control the matrix of indicator elements, and also the bus shapers — to obtain the prescribed electric characteristics of signals for indicator excitation [3]. Improvement of technical-and-economic characteristics and reliability parameters of such devices can be achieved, in the majority of realizations, through structural optimization of the functional network and of its individual units [10, 11]. In the case of scale-type indication devices, this problem is usually resolved by elaborating the signal processing algorithms and by selecting the most effective kinds of intermediate codes, generated in the digital part of the control network of IE matrix [12–14]. However, this approach to optimization of hardware decisions, despite its effectiveness, does not exhaust all opportunities for improvement technical-and-economic characteristics of discrete-analog indicator devices. The main disadvantage is "uniqueness" of the algorithm embedded in every specific hardware implementation.

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