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# IMPORTANCE OF THE "SECONDARY BREAKDOWN ENERGY" PARAMETER IN HIGH–POWER SWITCHING TRANSISTORS

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**The necessity in estimating the secondary breakdown energy of switching–type transistors is substantiated. The issues of improvement of reliability of high–power switching devices in bipolar transistors are considered.**

Experience in design and maintenance of high–power devices in bipolar transistors operating under switching conditions shows their low reliability. Failures of high–power transistors (HPT) may occur under conditions when maximum permissible steady–state parameters of current, voltage, and dissipated power are not exceeded, and the main cause of the HPT failure is the secondary breakdown [1, 2].

At the present time the HPT reliability is estimated mainly based on test results (for example, tests for longevity and no–failure operation) performed under dc conditions. In these situations, the reliability criteria do not consider the performance of HPT in switching devices, and the adopted system of powerful transistor parameters does not permit design of powerful switching devices meeting strict requirements for their reliability. There is a need for some additional parameter able to characterize the reliability of HPT in switching devices. Taking into account the fact that the main cause of HPT failure is the secondary breakdown (SB), it is expedient to introduce a parameter which can describe the immunity of transistors to secondary breakdown.

It should be noted that in switching devices the most essential limitations on the use of HPT are connected with secondary breakdown. It develops at the reverse bias of the emitter junction and is characterized in that it occurs at the stage of transistor switch–off because of two unfavorable factors: a so–called filament formation, i.e., constriction of the current into a string in the central part of the emitter due to voltage drop, across the distributed (ohmic) base resistance produced by the base inverse current; and large instantaneous power dissipated by the transistor because of energy supplied in the load inductance and in the parasitic inductance of the circuits.

Hence, this additional parameter has to characterize immunity of the transistor to the secondary breakdown under the reverse bias conditions of the emitter junction.

The most comprehensive information about a transistor's immunity to SB can be obtained from such energy characteristic as the energy of secondary breakdown (ESB) dissipated in the event of SB occurring in the structure. The magnitude of this energy characterizes the immunity of the transistor to secondary breakdown.

In order to have consistent data about a transistor's immunity to SB, we must use a unified method for ESB determination. It seems expedient to perform the tests of transistors with inductive load, when the transistor is most vulnerable to SB at the switch–off stage.

The transistor to be tested (TT) is connected as a common–emitter circuit. The control of TT switching is performed as follows. At first, by introducing a positive rectangular current pulse into the base, the transistor is put into saturation conditions with saturation current $I_{csat}$. Upon termination of the opening pulse, the TT passes from the saturation to the cutoff state, with the reverse bias in the transistor base circuit. Now the energy accumulated in the load inductance $L$, during

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