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INVESTIGATION OF DIGITAL SYSTEMS OF PHASE LOCKING WITH A DELAY IN THE CONTROL CIRCUIT

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Relationships have been derived defining the conditions of local stability of digital systems of phase locking with a delay in the control circuit. The principles of calculation of such systems with a prescribed duration of transient process are developed.

The potentialities of contemporary signal microprocessors open the possibility for wide application, in communication and data transmission equipment, of digital systems of phase locking (DSPL) able to realize various digital filtering algorithms. The output signal of such systems, with the aid of an analog-digital converter (ADC), with a clock frequency satisfying Kotelnikov's condition, is converted into digital form for all subsequent information processing in DSPL. The word-length of the input ADC is chosen based on permissible quantization error, so in the analysis of such systems they are considered discrete-type.

Mathematical models of DSPL with a delay in the control circuit are formed using the respective technical realizations. Particularly, the phase discriminator represents a combination of a multiplier and a low-pass filter, the latter providing for suppression of the double-frequency mode appearing at the multiplier output [1]. Moreover, in digital modems we can find some known algorithms for adaptive echo-cancellation with tracking the frequency detuning in the remote echo signal [2], etc.

The problems associated with analysis of such systems stem from a high order of the difference equation describing them. In the work below, based on the method of *D*-partition, we investigate the local stability (stability in a small neighborhood, to be exact) of DSPL with a delay of the *N*th order. We also suggest a method of calculation of the device parameters providing for a rough equivalence of duration of the transient processes that take place in them and in similar systems without delay.

Figure 1 shows the general block diagram of DSPL, which tracks the phase of a determinate quantized input action $u(k) = \sin(\omega_0 k + \Phi[k])$ where $\omega_0 = 2\pi f / f_d$, f and $\Phi[k]$ are the relative circular frequency, frequency, and phase of the controlling oscillation, respectively; f_d is the quantization frequency; and k is the number of the signal sample.

The block diagram shown includes a phase discriminator with sinusoidal nonlinearity, providing at its output the instantaneous phase difference $\psi[k] = \Phi[k] - \hat{\Phi}[k]$ between the controlling $\Phi[k]$ and tuned $\hat{\Phi}[k]$ oscillation, and contains also a delay by N quantization cycles and a filter with its transfer function $H_\Phi(z)$. The form of $H_\Phi(z)$ is defined by the digital filtration algorithm employed in the system. For the DSPL under analysis we shall use the algorithm of the 2nd order discrete astatic system of phase adjustment described by the difference equation

$$\hat{\Phi}[k] = 2 \cdot \hat{\Phi}[k-1] - \Phi[k-2] + k1 \cdot \Delta\varphi[k-1] + k2 \cdot \Delta\varphi[k-2]$$

where $\Delta\varphi[k] = \sin(\psi[k])$ is the signal magnitude at the phase discriminator output without taking noise into account; $k1$ and $k2$ are constant coefficients defining the system characteristics.

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